

## CLAIMS

What is claimed is:

- 1 1. An apparatus, comprising:  
2 an input-output interface to receive a first transaction associated with a  
3 first address;  
4 an address queue coupled with said input-output interface to store a second  
5 address of a pending transaction;  
6 address logic circuitry coupled with said address queue to compare the  
7 first address against the second address; and  
8 ownership pre-fetch circuitry coupled with said address logic circuitry to  
9 initiate a request for an ownership of a first memory content  
10 associated with the first address for the first transaction unless the  
11 first address is substantially equivalent to the second address.
- 1 2. The apparatus of claim 1, further comprising a transaction queue coupled with  
2 said input-output interface to store a header for the pending transaction.
- 1 3. The apparatus of claim 1, further comprising a cache coupled with said input-  
2 output interface to store data of a memory line to anticipate a subsequent read  
3 transaction.
- 4 4. The apparatus of claim 3, further comprising read logic circuitry coupled with said  
5 input-output interface to attach cache line invalidation data to another read  
6 transaction to invalidate the read data.
- 1 5. The apparatus of claim 1, further comprising transaction bypass circuitry coupled  
2 with said input-output interface to allow the first transaction to advance upbound  
3 substantially independent of an advancement of the pending transaction, wherein  
4 the first address is different from the second address.

- 1 6. The apparatus of claim 5, wherein the transaction bypass circuitry comprises  
2 transaction bypass circuitry coupled with said input-output interface to the first  
3 transaction to advance upbound substantially independent of an advancement of  
4 the pending transaction, wherein a memory line address associated with the first  
5 transaction is different from a memory line address associated with the pending  
6 transaction.
- 1 7. The apparatus of claim 5, wherein the transaction bypass circuitry comprises  
2 transaction bypass circuitry coupled with said input-output interface to allow the  
3 first transaction to advance upbound substantially independent of an advancement  
4 of the pending transaction, wherein a first hub identification associated with the  
5 first transaction is different from a second hub identification associated with the  
6 pending transaction.
- 1 8. The apparatus of claim 1, wherein said input-output interface comprises circuitry  
2 to transmit and receive data from an input-output device.
- 1 9. The apparatus of claim 1, wherein said address queue comprises circuitry to  
2 associate the second address with the pending transaction.
- 1 10. The apparatus of claim 9, wherein the circuitry comprises memory to store an  
2 association with an entry in a transaction queue.
- 1 11. The apparatus of claim 1, wherein said address logic circuitry comprises circuitry  
2 to compare the first address against an invalidation address associated with the  
3 pending transaction to prevent the first transaction from bypassing the pending  
4 transaction, wherein the invalidation address is substantially equivalent to the first  
5 address.

1 12. The apparatus of claim 1, wherein said ownership pre-fetch circuitry comprises  
2 circuitry to initiate the request for the ownership before a transaction order of the  
3 first transaction is to satisfy an ordering rule.

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- 1 13. A method, comprising:  
2 receiving a first transaction from an ordered interface;  
3 comparing a first address associated with the first transaction against a  
4 second address in an address queue, wherein the second address is  
5 associated with a second transaction; and  
6 pre-fetching ownership of a memory content associated with the first  
7 address, wherein the first address is different from the second  
8 address.
- 1 14. The method of claim 13, further comprising comparing the first address to a  
2 cached address associated with a line of a cache, wherein the first transaction  
3 comprises a read transaction.
- 1 15. The method of claim 14, further comprising responding to the first transaction  
2 with the line of the cache, wherein the first address substantially matches the  
3 cached address.
- 1 16. The method of claim 14, further comprising attaching cache line invalidation data  
2 to the read transaction to invalidate the line of the cache.
- 1 17. The method of claim 13, further comprising advancing the first transaction to an  
2 unordered interface substantially independent of an advancement of the second  
3 transaction to the unordered interface, wherein the first address is different from  
4 the second address.
- 1 18. The method of claim 17, wherein advancing the first transaction comprises  
2 advancing a read transaction.
- 1 19. The method of claim 18, wherein advancing the first transaction comprises  
2 advancing a read transaction to the unordered interface substantially independent  
3 of the advancement of the second transaction unless a memory line address

4 associated with the read transaction is substantially equivalent to a memory line  
5 address associated with the second transaction.

1 20. The method of claim 17, wherein advancing the first transaction comprises  
2 advancing the first transaction to the unordered interface substantially independent  
3 of the advancement of the second transaction, wherein a hub identification  
4 associated with the second transaction is different from a hub identification  
5 associated with the first transaction.

1 21. The method of claim 13, wherein said comparing a first address comprises  
2 comparing a first memory line address associated with the first transaction against  
3 a second memory line address associated with the second transaction.

1 22. The method of claim 13, wherein said comparing a first address comprises  
2 comparing a first hub identification of the first address against a second hub  
3 identification of the second address.

1 23. The method of claim 13, wherein said pre-fetching ownership comprises initiating  
2 a request for ownership of the memory content by the first transaction before the  
3 second transaction is to satisfy an ordering rule to transmit to the unordered  
4 interface.

1 24. A system, comprising:  
2 an input-output interface to receive a first transaction associated with a  
3 first address;  
4 an address queue coupled with said input-output interface to store a second  
5 address of a pending transaction;  
6 address logic circuitry coupled with said address queue to compare the  
7 first address against the second address;  
8 ownership pre-fetch circuitry coupled with said address logic circuitry to  
9 initiate a request for an ownership of a first memory content  
10 associated with the first address for the first transaction, wherein  
11 the first address is different from the second address;  
12 a transaction queue coupled with said input-output interface to maintain a  
13 transaction order for the pending transaction; and  
14 a memory device coupled with said transaction queue to respond to the  
15 pending transaction.

1 25. The system of claim 24, further comprising a scalability port switch coupled with  
2 said transaction queue to transmit the pending transaction to said memory device.

1 26. The system of claim 24, further comprising a bridge coupled with said input-  
2 output interface to couple more than one input-output device with said input-  
3 output interface.

1 27. A machine-readable medium containing instructions, which when executed by a  
2 machine, cause said machine to perform operations, comprising:  
3 receiving a first transaction from an ordered interface;  
4 comparing a first address associated with the first transaction against a  
5 second address in an address queue, wherein the second address is  
6 associated with a second transaction; and  
7 pre-fetching ownership of a memory content associated with the first  
8 address, wherein the first address is different from the second  
9 address.

1 28. The machine-readable medium of claim 27, further comprising comparing the first  
2 address to a cached address associated with a line of a cache, wherein the first  
3 transaction comprises a read transaction.

4 29. The machine-readable medium of claim 27, wherein said comparing a first  
5 address comprises comparing a first hub identification of the first address against  
6 a second hub identification of the second address.

1 30. The machine-readable medium of claim 27, wherein said pre-fetching ownership  
2 comprises initiating a request for ownership of the memory content by the first  
3 transaction.